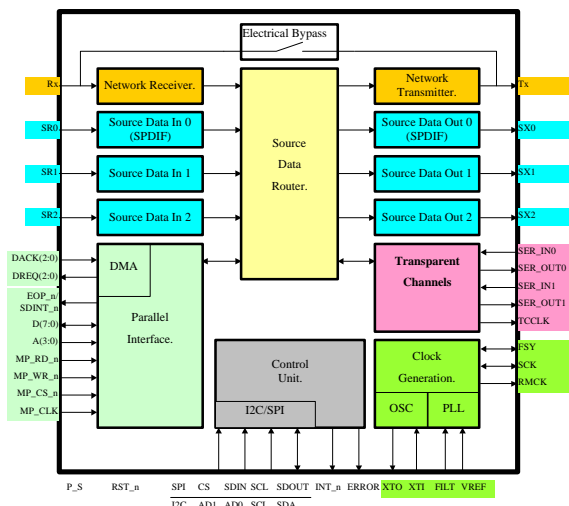


Product Datasheet 2.2.0

Preliminary

Super Conan[®] DMA



- Fully compliant with D2B Optical Mode0 and Mode1 Protocol
- Simultaneous transfer of Voice and Graphics for advanced GPS Navigation Systems
- Multiple synchronous data channels via three serial ports
- Asynchronous data Transfer capability via DMA or interrupt driven parallel interface ports.
- Flexible sharing of data capacity between serial/parallel interfaces
- Full range of D2B APIs for in-car AV and ITS devices with easy implementation of proprietary control messaging supported

THE D2B OPTICAL PROTOCOL

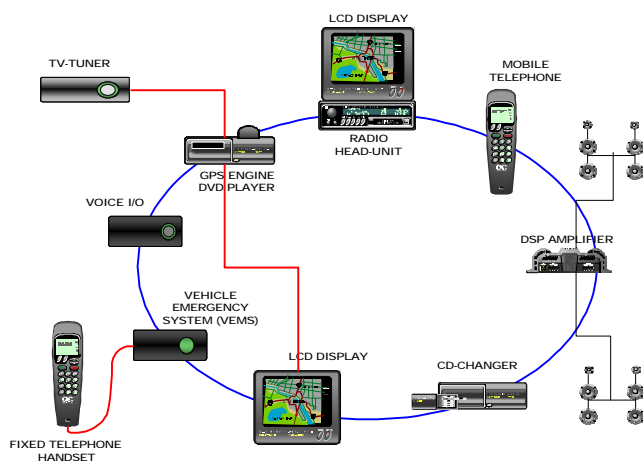
The Digital Data Bus (D2B Optical) is a networking protocol for automotive multimedia data communication integrating digital audio, video and other high data rate synchronous or asynchronous signals, with the control data for network management protocols and APIs. The protocol enables robust single cable interconnection and compatible interoperability of in-car AV multimedia and ITS devices, such as Radio Head Units, CD Changer, CD-ROM, GPS Navigation, Voice Control, Car Telephones, TV and others.

SUPER CONAN[®]

The SCI8001 is an advanced CMOS device which supports D2B Optical Mode0 and Mode1 protocol and enables full backwards compatible operation in multimedia networks using CONAN[®] -- OCC8001 devices which support D2B Optical Mode0 only.

SERIAL SOURCE DATA

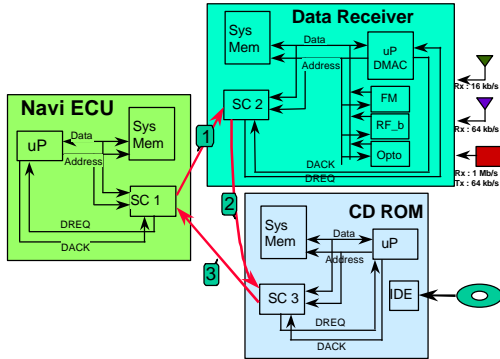
Super CONAN[®] handles multiple synchronous source data channels from 1,4 Mbps up to a maximum of 10.75Mbps for the transfer of MPEG2 encoded video data. Through three source data input ports (SR0-2) and three output ports (SX0-2) one Super CONAN[®] IC can flexibly process multiple data sources and destinations. All data ports share a common frame synchronization and serial bit clock. Data can be arranged as either Philips I2S, Sony or Matsushita, 16 or 24 bit serial formats. Additionally, SR/X0 can be configured for operation as an IEC-958 (SPDIF) serial interface.



CONTROL PORT

Control of the Super CONAN® IC can be via the parallel interface or by an I2C or SPI compatible control port.

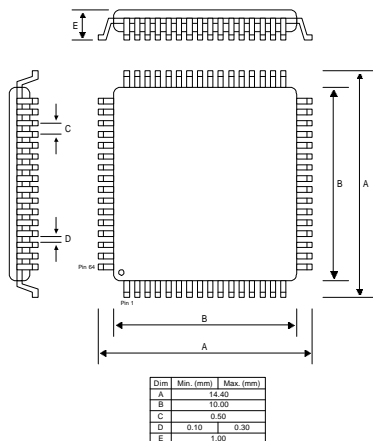
PARALLEL INTERFACE



Navigation Application

The 8 bit wide parallel interface for source and control data incorporates two 28 byte buffers, which perform rate conversion between data from the network and data from the application.

One buffer handles data from the network, whilst the other handles data from the application. After each frame, the buffers swap over, allowing current data to be read by the application or transmitted on the network and new data to be loaded.



Super CONAN® Package Outline

The parallel interface (PI) supports synchronous and asynchronous data rates of 10.36Mbit/s. It can be driven on an interrupt or polled basis, or via DMA data transfer.

The DMA transfer is compatible with industry standard microprocessors and DMA controllers such as Intel 8237A, Hitachi SH7604. The PI provides three DMA channels with the ability to read and write with each channel concurrently without reconfiguring the DMA controller and supports single, block and demand DMA modes controller operation

D2B Optical Protocol		Mode0 & Mode1
Data Rate @ f_s 48kHz		
▪ Gross Data Rate		Max. 24.58 Mb/s
▪ Synchronous Data		Max. 10.75 Mb/s
▪ Asynchronous Data		Max. 10.36Mb/s
▪ Control Data		Max. 192 Kb/s
Line Coding		Manchester
Topology		Ring
Max. nr. of Nodes		24
Ultra Low Jitter		>80pS/node
Control Port	I ² C	400 kHz
	SPI	2 MHz
Parallel Interface		For μ P data busses >8bit
DMA		3 Channels-Duplex Transmission
ESD Protection		+/- 4 kV HB model +/- 400 V M model
Power Consumption		300 mW at +3.3V
Supply Voltage		3.3V \pm 10%
Temperature Range		-40°C to +85°C
Package		64 QFP

Order-information for the Super Conan® DMA

Part: Super Conan SCI8001 Order number: 2-02-001-01

For further information on any other C&C Electronics products, please visit our Web site or contact us:

<http://www.candc.co.uk>

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