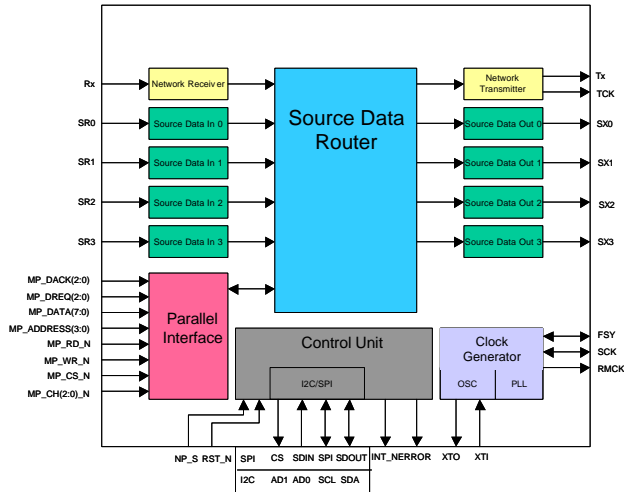


# MegaCONAN<sup>®</sup> Media Access Controller. Product Brief.



- Up to 24.58Mb/s source data rate at a sampling frequency,  $f_s=48\text{kHz}$  (22.58 Mb/s at  $f_s=44.1\text{kHz}$ )
- Flexible mix of parallel & serial source data channels.
- SPDIF audio port.
- Automatic simultaneous operation 44.1kHz and 48kHz sample rate audio devices.
- I2C or SPI compatible serial, or parallel control port available.
- Parallel microprocessor interface port for control and source data.
- Asynchronous source data capability via parallel interface with internal 3x1k byte buffers.
- Power requirements, less than 500mW @ 3.3V
- Operation over automotive temperature range.

## General Description.

The MegaCONAN<sup>®</sup> technology is a further step in the development of communication networks for automotive multimedia applications. The MegaCONAN<sup>®</sup> Transceiver enhances network design by integrating source data, such as digital audio, video and other high rate digital data, with the control data for communication management. The MegaCONAN<sup>®</sup> is designed to operate with

either the D2B Smartwire or Plastic Optical Fibre (POF) physical layer to give high real-time data capacity and immunity to interference and noise. The MegaCONAN<sup>®</sup> IC handles multiple source data channels via common serial interface standards or a parallel processor interface. Control of the MegaCONAN<sup>®</sup> IC can be via the parallel interface or by the I2C/SPI serial control port.

Features	Benefits
<ul style="list-style-type: none"> <li>• Integration of source and control data.</li> <li>• Multiple source data channels.</li> <li>• Parallel, buffered interface.</li> <li>• Multiple source data formats.</li> <li>• High source data capacity.</li> <li>• Flexible source data routing.</li> <li>• Loss less rate matching in audio ports.</li> <li>• Programmable clock manager.</li> <li>• Low jitter PLL.</li> <li>• Versatile control messaging.</li> </ul>	<ul style="list-style-type: none"> <li>• Reduces the number of components required for signal distribution and control.</li> <li>• Allows simultaneous bi-directional transmission of up to 4 source data channels, using a single MegaCONAN<sup>®</sup> IC.</li> <li>• Allows flexible integration with microprocessors, including data buses greater than 8 bits.</li> <li>• Adaptability to a variety of components which support different digital data formats.</li> <li>• Allows transport of MPEG2 encoded digital video data.</li> <li>• Versatile use of the network capacity.</li> <li>• Allow mixed rate audio devices to operate simultaneously without loss of quality.</li> <li>• Easy integration in different products.</li> <li>• Low jitter ensures low bit error rate and high network reliability.</li> <li>• Different addressing methods (incl. broadcast) make best use of control channel capacity.</li> </ul>

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## Network Interface.

Data is transported on the network in frames. Frames are circulated at 48kHz. Lower data rate audio data is accommodated using a loss less rate adaptation algorithm. At a sampling frequency,  $f_s$ , of 48kHz, the source data rate is 24.58Mb/s. Control data is constructed into a control frame, which is transferred at a rate of two bytes per frame. The control frame comprises 256 bits and requires a block of 32 frames to transmit.

## Serial Source Data Ports.

8 serial source data ports are provided for normal source data mode, four input (SR0-2) and four output (SX0-2), giving flexibility for multiple data sources and destinations to be handled by one MegaCONAN<sup>®</sup> IC.

Data can be arranged as Philips I2S, Sony or Matsushita, 16 or 24 bit serial formats. Additionally, SR0/SX0 can be configured for operation as an IEC-958 (SPDIF) serial interface.

The serial source data ports automatically perform sample rate matching through a virtual variable rate channel between MegaCONAN<sup>®</sup> devices.

The serial source port may also be used to transfer RS232 type data.

## Serial Control Interface.

In serial mode, the control port can be configured as either an I2C or SPI compliant interface. The interface type is selected during a hardware reset.

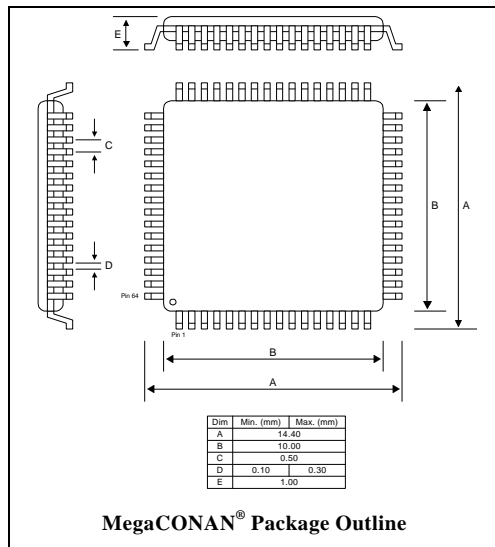
## Parallel Interface With DMA.

The parallel interface can be driven on an interrupt or polled basis, or via DMA data transfer.

## System Clock Management.

The MegaCONAN<sup>®</sup> IC needs a clock source to generate the timing of internal and external (network) communication. In master mode the MegaCONAN<sup>®</sup> device generates the timing for the whole network. The clock can be derived from a crystal or an external clock. In slave mode, the MegaCONAN<sup>®</sup> device recovers the clock from the incoming network bit stream.

The on-chip PLL generates the user programmable output clock (RMCK) for use by the application circuit.



For further information on the MegaCONAN<sup>®</sup> IC, or any other C&C Electronics products, please visit our Web site or contact our head office.

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